

FIG. 1A

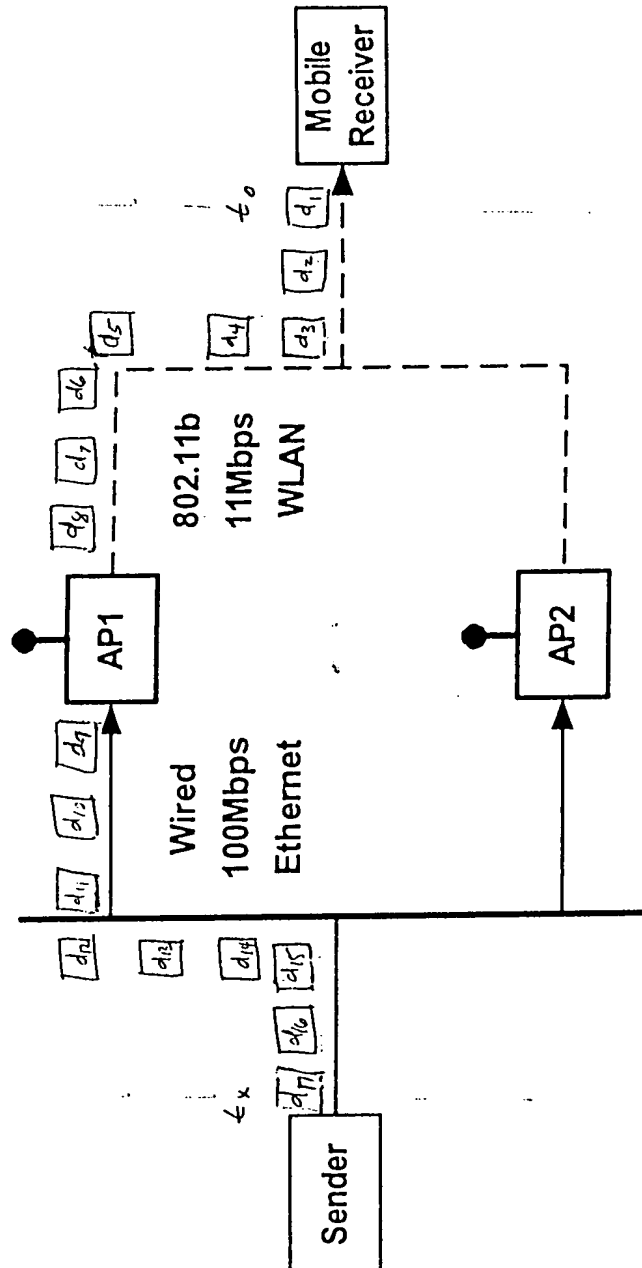


FIG. 1B

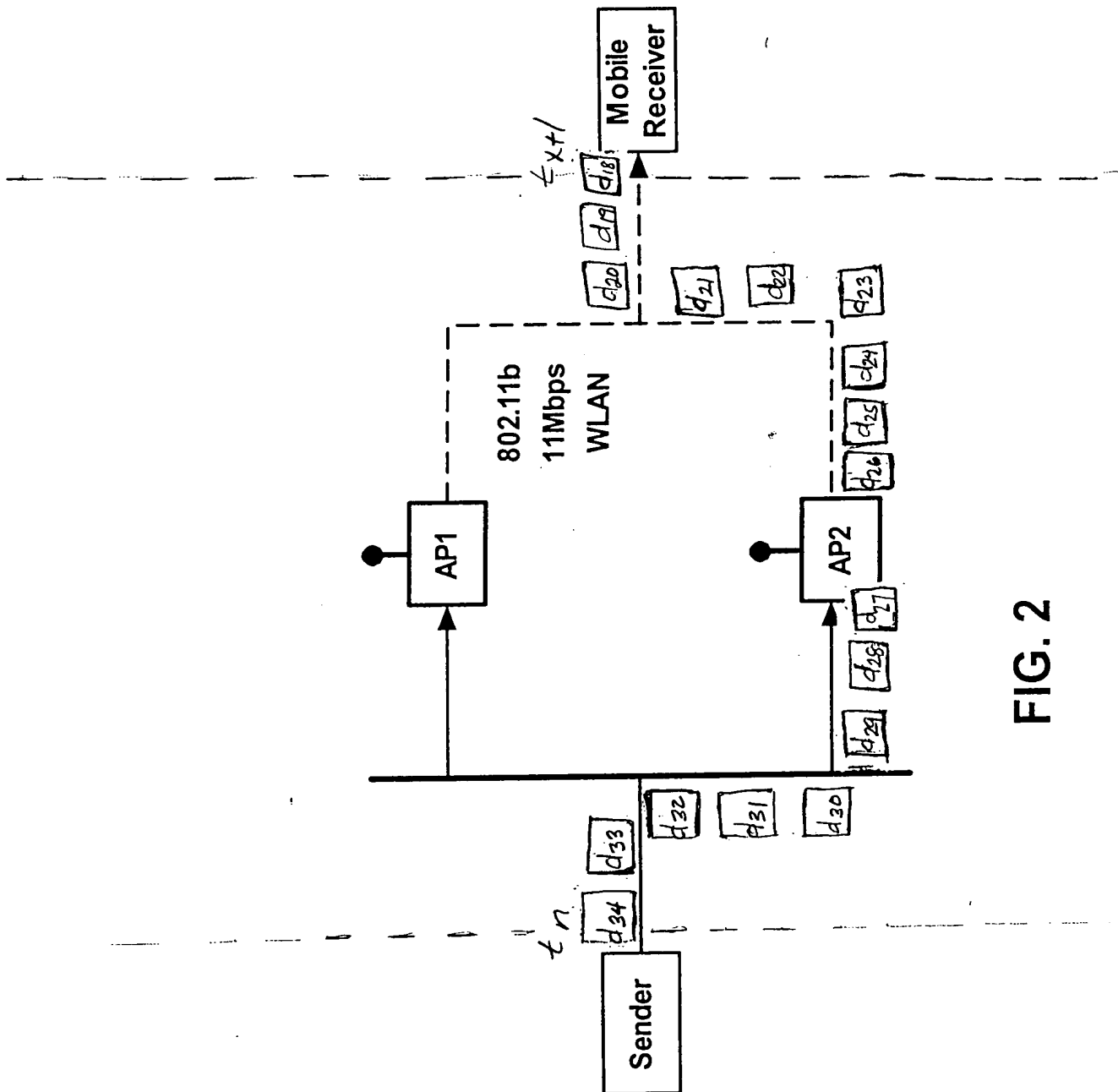


FIG. 2

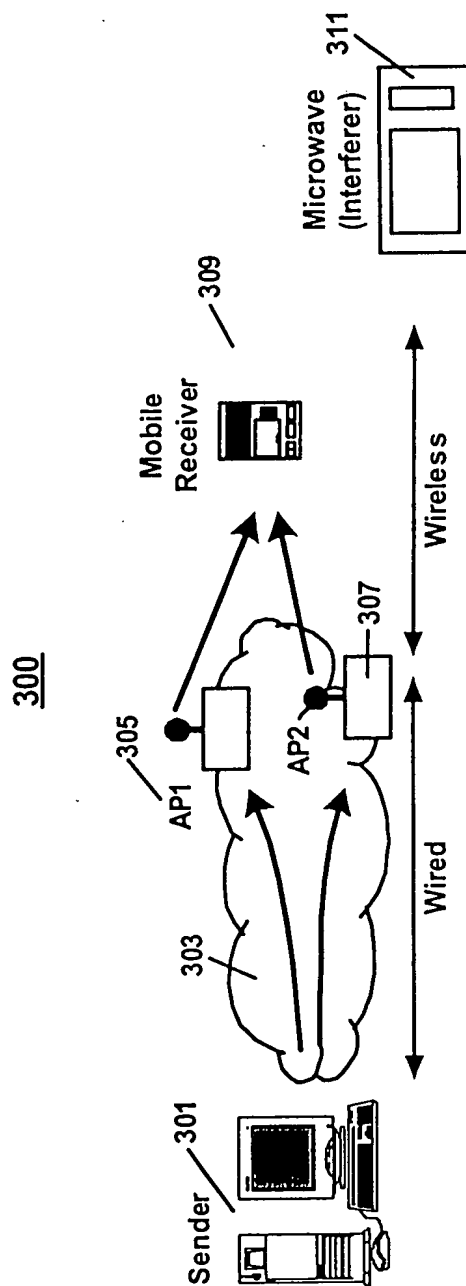


FIG. 3

FIG. 4A

300

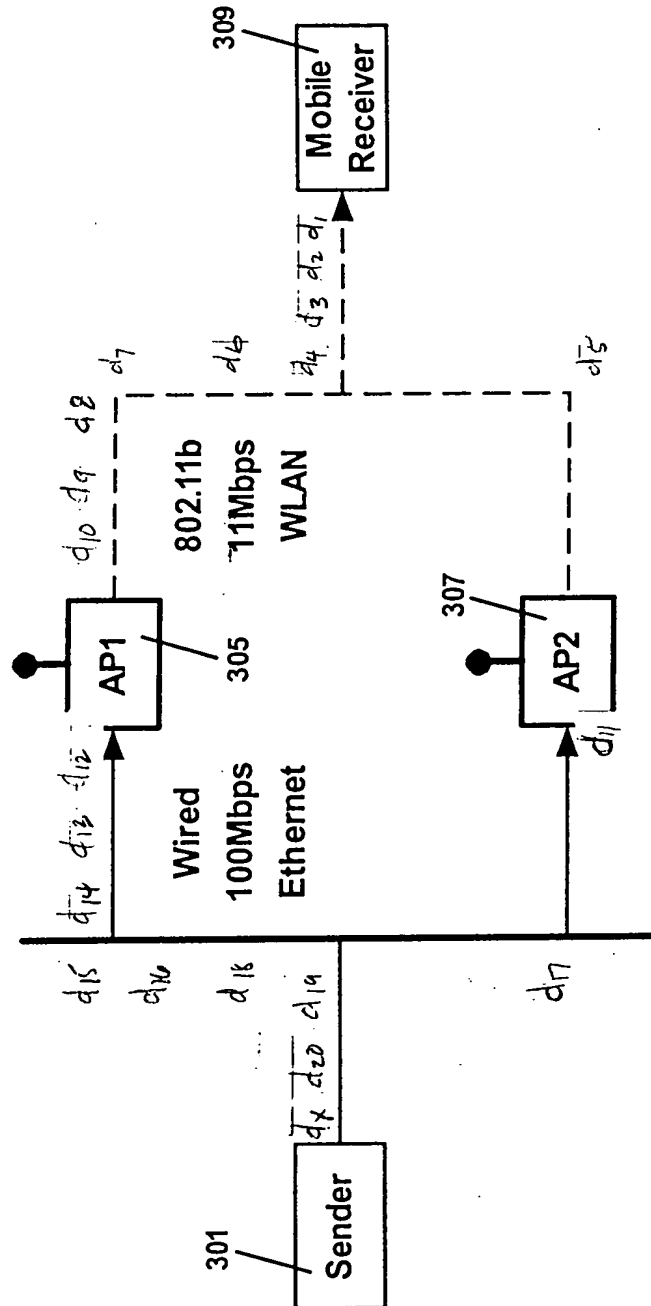


FIG. 4B

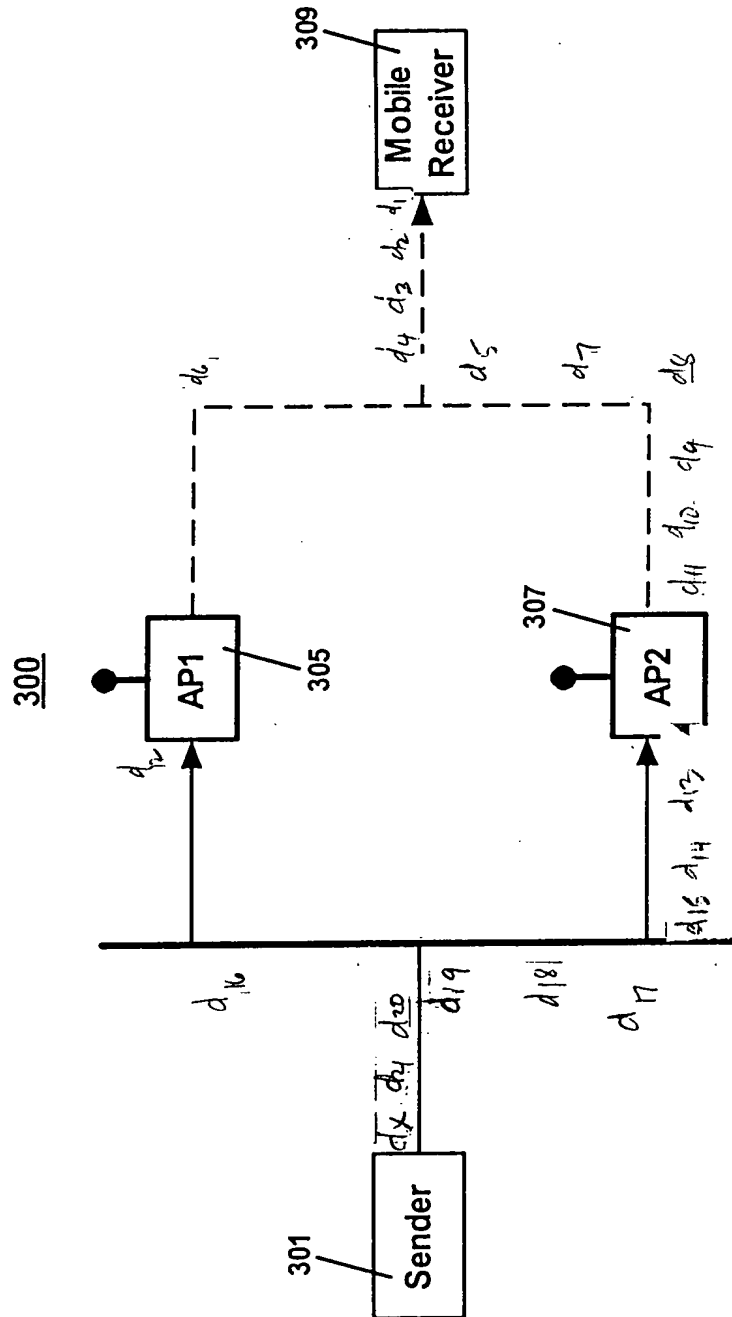


FIG. 4C

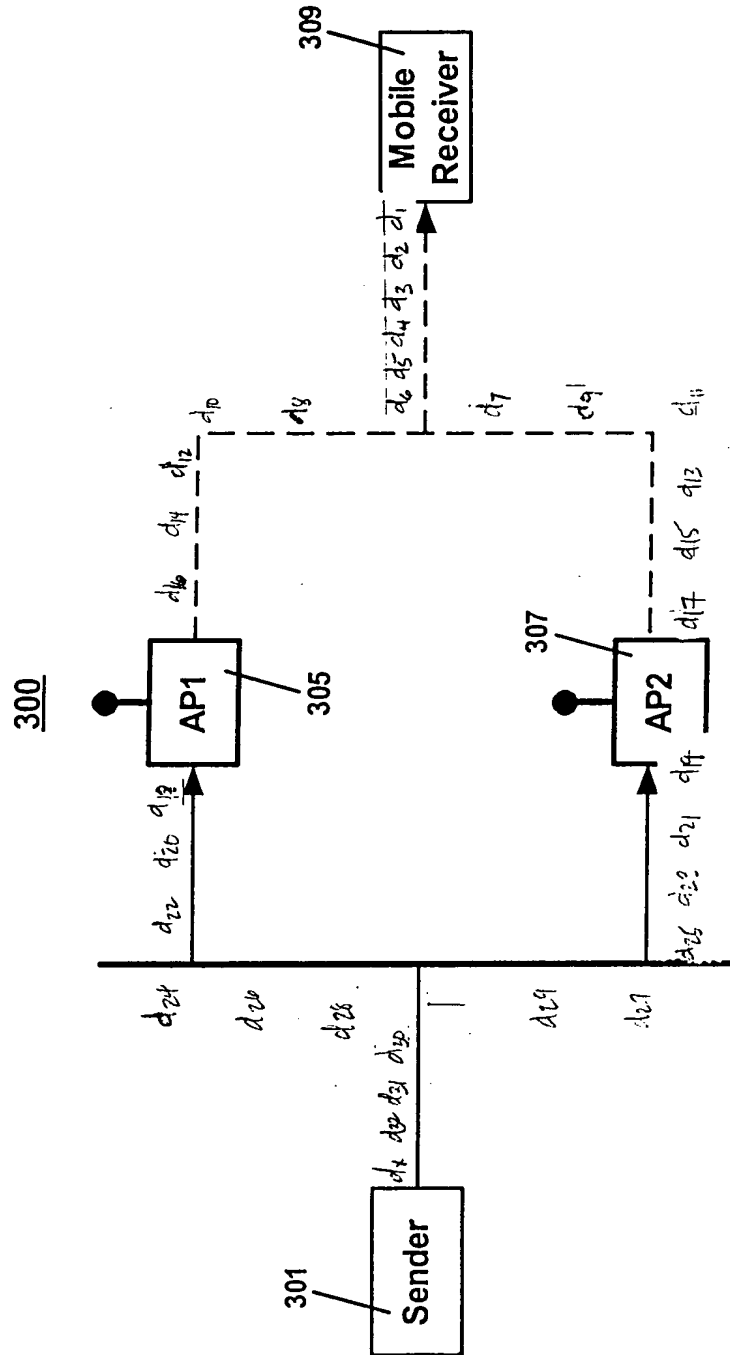


FIG. 4D

500

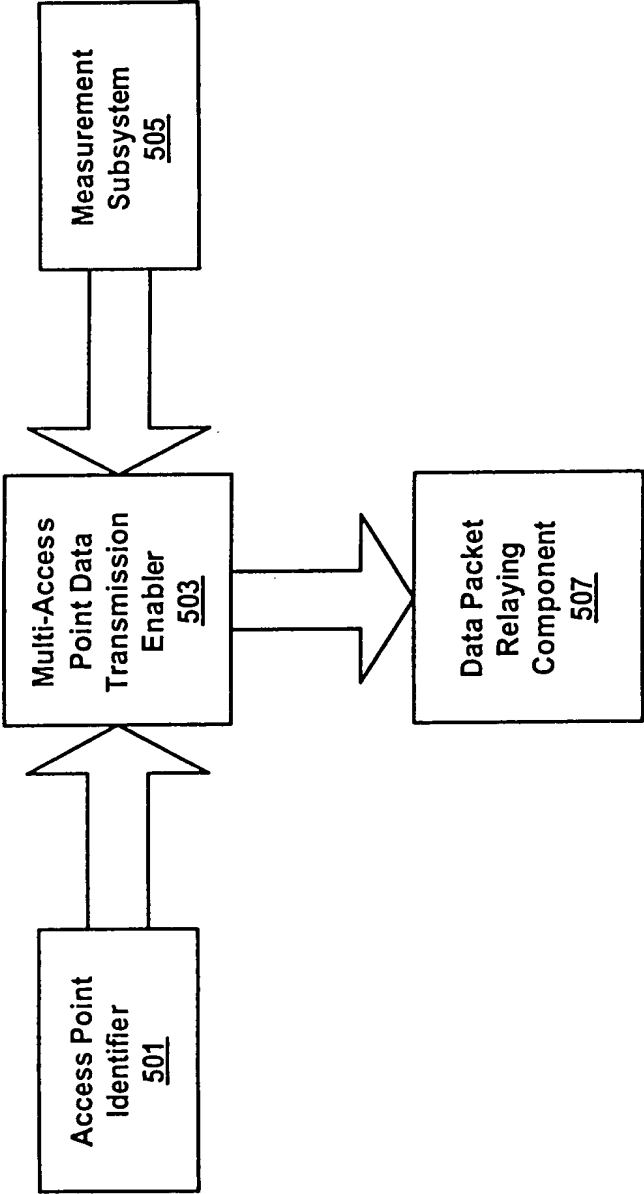


FIG. 5

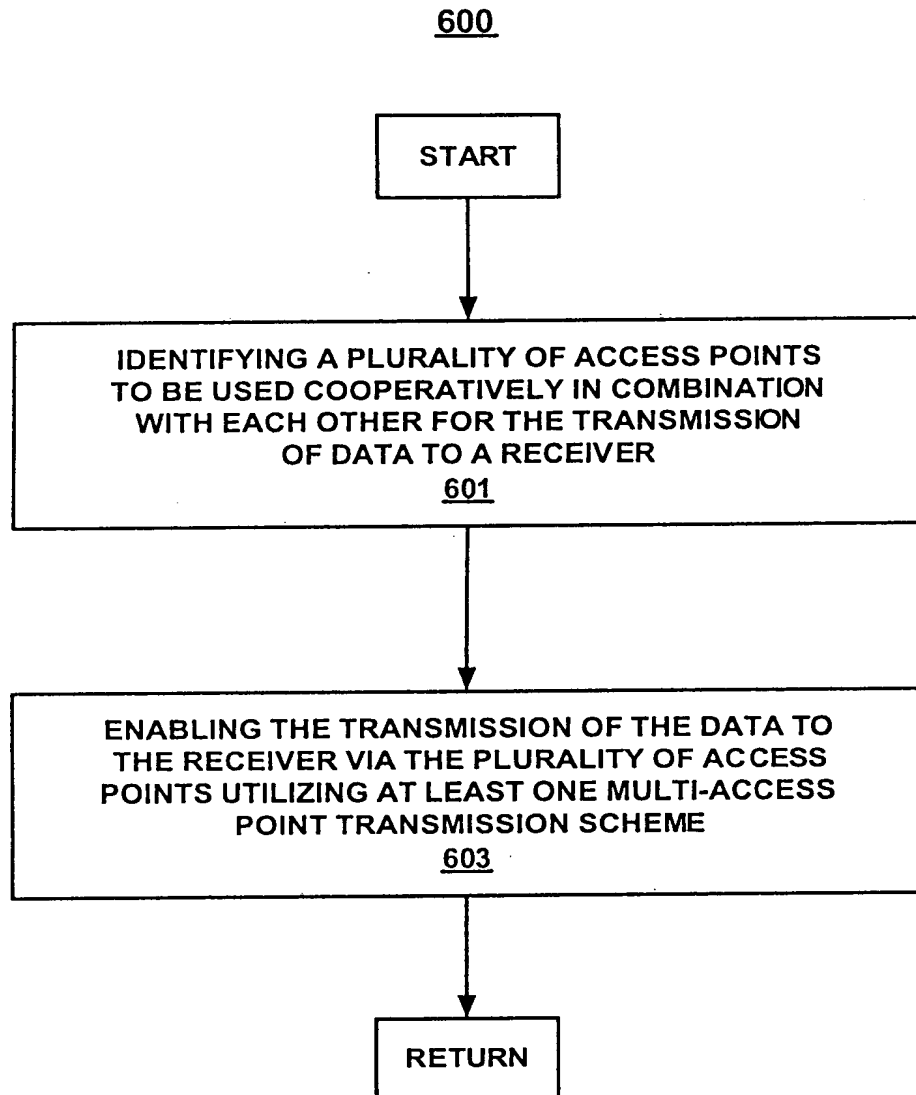


FIG. 6

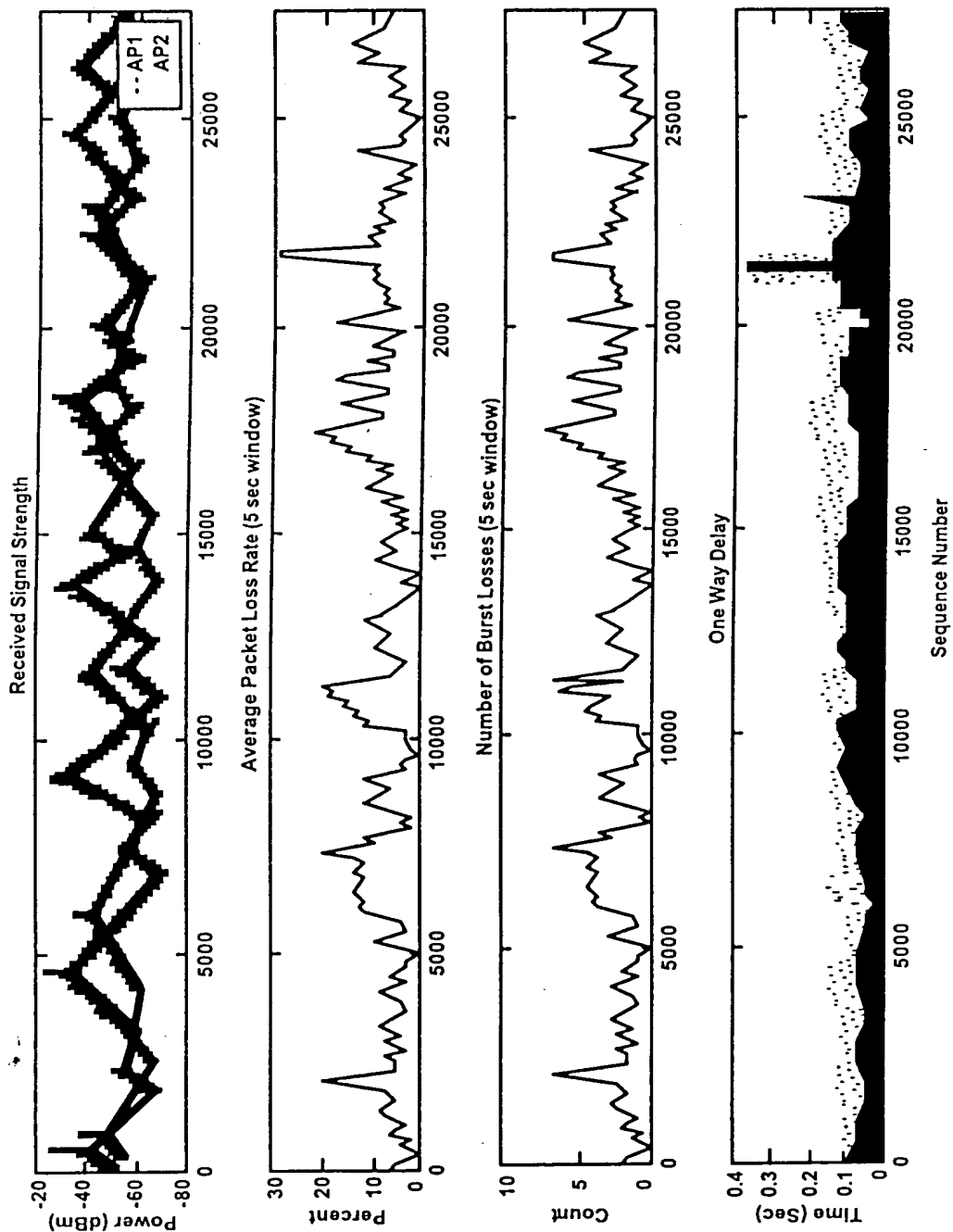


FIG. 7

Table 1.

Scheme	Delay Threshold (D_{thr})									
	40ms			80ms			∞			
	PLR	PLR _B	Bursts	PLR	PLR _B	Bursts	PLR	PLR _B	Bursts	
AP1	16.41	11.97	956	8.32	4.98	386	6.56	2.86	288	
AP2	18.20	13.29	1074	9.00	5.32	415	7.00	3.01	323	
Balanced	17.19	5.48	545	8.58	1.45	131	6.70	0.63	67	
Site Selection	13.89	9.01	818	6.00	2.74	243	4.58	1.35	144	
Oracle	3.73	2.06	184	0.92	0.59	38	0.26	0.13	9	

FIG. 8

Table 2.

Scheme	Sequence							
	Foreman (35.8 dB at 156.2 kb/s)		Claire (39.6 dB at 39.2 kb/s)		Mother & Daughter (36.2 dB at 68.6 kb/s)		Salesman (34.9 dB at 67.6 kb/s)	
	PSNR _{Avg}	N_{thresh}	PSNR _{Avg}	N_{thresh}	PSNR _{Avg}	N_{thresh}	PSNR _{Avg}	N_{thresh}
AP1	24.34	71	31.61	8	31.23	15	30.19	16
AP2	24.01	69	31.05	9	31.12	17	29.85	10
Balanced	24.40	82	32.78	6	31.81	9	30.76	7
Site Selection	25.77	58	34.11	2	32.79	4	32.03	3
Oracle	31.58	7	37.11	1	35.12	2	33.92	2

FIG. 9

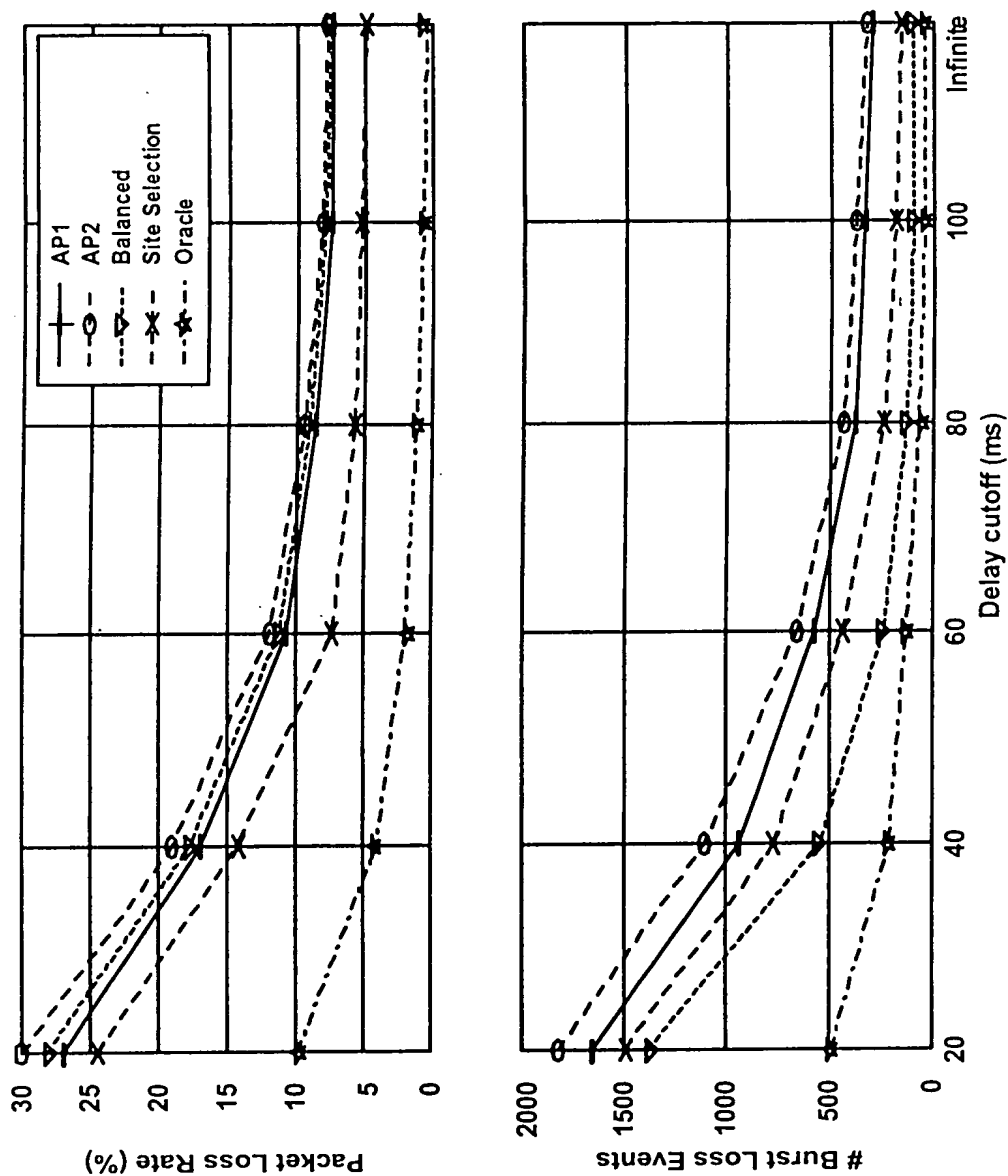


FIG. 10A

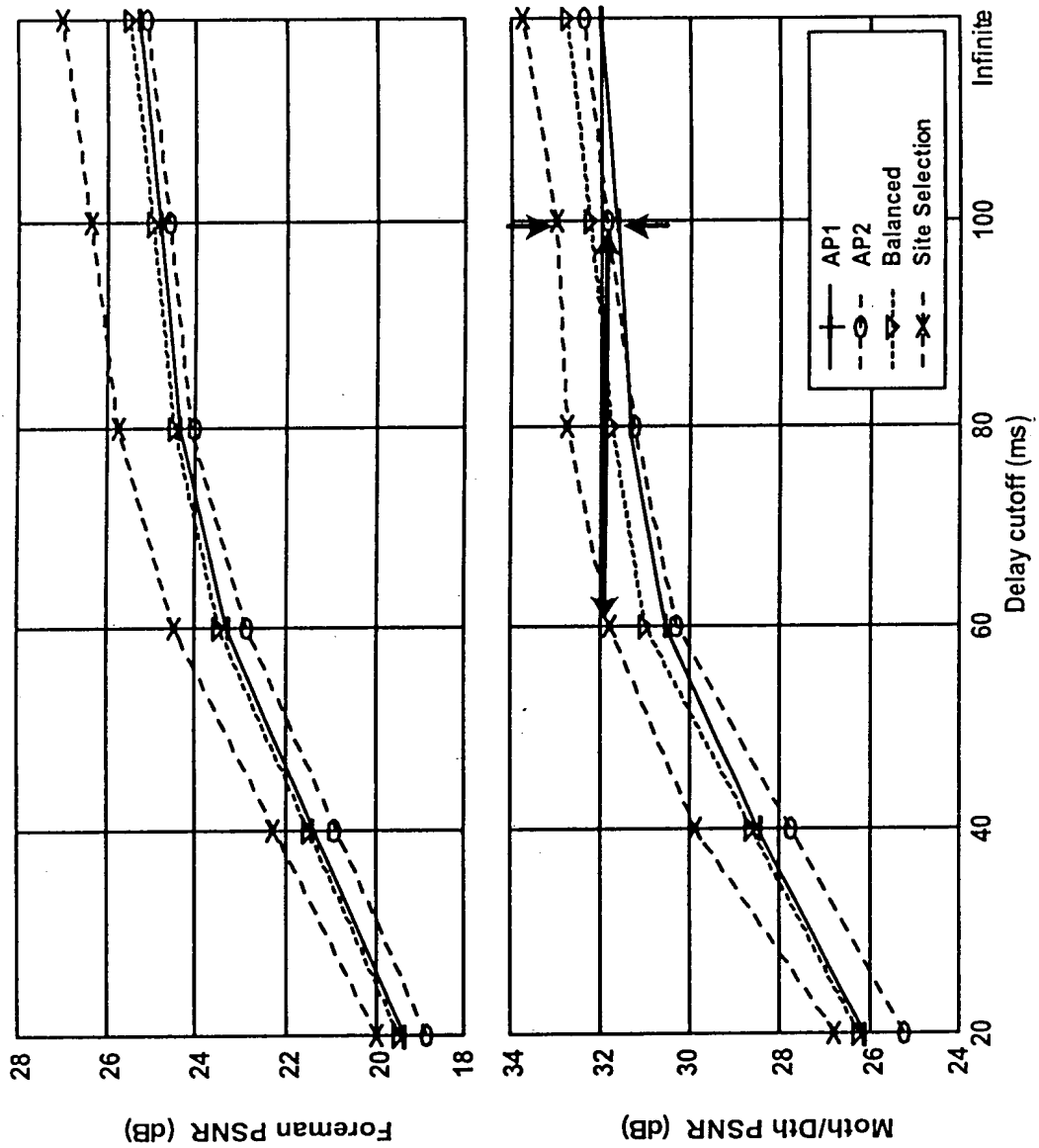


FIG. 10B